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- IEEE JNL IEEE Journal or Magazine
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Giorgetti, N.; Pappas, G.J.; Bemporad, A.;
Decision and Control, 2005 and 2005 European Control Conference. CDC-ECC '05. 44th IEEE Conference on
12-15 Dec. 2005 Page(s):672 - 677
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Schuele, T.; Schneider, K.;
Formal Methods and Models for Co-Design, 2004. MEMOCODE '04. Proceedings. Second ACM and IEEE International Conference on
23-25 June 2004 Page(s):17 - 26
Digital Object Identifier 10.1109/MEMCOD.2004.1459809
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Katz, J.; Hanna, Z.; Dershowitz, N.;
Design, Automation and Test in Europe, 2005. Proceedings
2005 Page(s):686 - 687 Vol. 2
Digital Object Identifier 10.1109/DATE.2005.276
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Shacham, O.; Zarpas, E.;
Microprocessor Test and Verification: Common Challenges and Solutions, 2003. Proceedings. 4th International Workshop on
29-30 May 2003 Page(s):75 - 79
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- ☐ 5. **Can BDDs compete with SAT solvers on Bounded Model Checking?**
Cabodi, G.; Camurati, P.; Quer, S.;
Design Automation Conference, 2002. Proceedings. 39th
10-14 June 2002 Page(s):117 - 122
Digital Object Identifier 10.1109/DAC.2002.1012605
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[IODINE: a tool to automatically infer dynamic invariants for hardware designs](#)

 Sudheendra Hangal, Naveen Chandra, Sridhar Narayanan, Sandeep Chakravorty
 June 2005 **Proceedings of the 42nd annual conference on Design automation**

Publisher: ACM Press

 Full text available: pdf(630.99 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

We describe IODINE, a tool to automatically extract likely design properties using dynamic analysis. A practical bottleneck in the formal verification of hardware designs is the need to manually specify design-specific properties. IODINE presents a way to automatically extract properties such as state machine protocols, request-acknowledge pairs, and mutual exclusion between signals from design simulations. We show that dynamic invariant detection for hardware designs can infer relevant and accurate ...

Keywords: dynamic analysis, dynamic invariants, formal specification

122 [SAT: cool algorithms and hot applications: Efficient SAT solving: beyond supercubes](#)



Domagoj Babić, Jesse Bingham, Alan J. Hu

 June 2005 **Proceedings of the 42nd annual conference on Design automation**

Publisher: ACM Press

 Full text available: pdf(603.26 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

SAT (Boolean satisfiability) has become the primary Boolean reasoning engine for many EDA applications, so the efficiency of SAT solving is of great practical importance. Recently, Goldberg *et al* introduced *supercubing*, a different approach to search-space pruning, based on a theory that unifies many existing methods. Their implementation reduced the number of decisions, but no speedup was obtained. In this paper, we generalize beyond supercubes, creating a theory we call *B-cubi* ...

Keywords: SAT, formal verification, learning, search space pruning

123 [Effective formal verification using word-level reasoning, bit-level generality, and](#)



[parallelism: Word level predicate abstraction and refinement for verifying RTL verilog](#)

Himanshu Jain, Daniel Kroening, Natasha Sharygina, Edmund Clarke

 June 2005 **Proceedings of the 42nd annual conference on Design automation**

Publisher: ACM Press

 Full text available: pdf(601.22 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Model checking techniques applied to large industrial circuits suffer from the state space explosion problem. A major technique to address this problem is abstraction. The most